

REMARKS

This section will address the 35 USC 112, 35 USC 102, and 35 USC 103 rejections of the Office Action of November 19, 2003.

A. Status of the Claims

Claims 1, 30, and 40 are objected to. Claims 1-5, 7-14, 30-34, 36-48, and 50-62 have been rejected under 35 USC 112. Claims 1, 7-9, 11, 12, 14, 30, 36-42, 44, 50, 51-53, 54 and 60-62 have been rejected under 35 USC 102. Claims 2-5, 13, 31-34, 42, 45-48, and 55 have been rejected under 35 USC 103.

B. Objections

Claims 1, 30, and 40 were objected to. In claim 1, the Examiner directed that the modifying word "polysilicon", which modified the first occurrence of the term "semiconductor regions", be included in subsequent occurrences of the same term. Similarly, in claim 30, the Examiner wished the modifying word "polysilicon", which modified the first occurrence of the term "regions", to be included in subsequent occurrences of the same word. These modifications have been made in this amendment and response.

The Examiner also objected to claim 40, but did not specify the objection or a remedy; thus no amendment to claim 40 was made.

C. 35 USC 112 Rejections

Claims 1-5, 7-14, 30-34, 36-48, and 50-62 have been rejected under 35 USC 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Specifically, the Examiner writes:

It is not known what is the width that "a first width" referring to.

Should the first width be the width of the wafer or the width of the semiconductor regions or the width of the dielectric regions?

Claim 1 recites a wafer having a surface, the wafer comprising a plurality of regions of dielectric and polysilicon semiconductor exposed at the surface of the wafer after chemical mechanical planarization, the polysilicon semiconductor regions formed over a substrate, wherein the polysilicon semiconductor regions have a total surface area

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that is less than or equal to a first fraction of a total surface area of the wafer and each of the polysilicon semiconductor regions have a **shortest surface dimension that is less than or equal to a first width**, the first fraction and the first width ensuring that the surface of the wafer can attract enough water to wet sufficiently allowing removal of residual particles therefrom, and wherein the surface is planarized.

The relevant language, bolded above, is as follows: "... each of the polysilicon semiconductor regions have a shortest surface dimension that is less than or equal to a first width, ... the first width ensuring that the surface of the wafer can attract enough water to wet sufficiently allowing removal of residual particles therefrom ..."

Recall that the invention relates to wet cleaning of wafer surfaces following chemical mechanical planarization (CMP). An aqueous cleaning technique is conventionally used to remove residual slurry particles from a silicon dioxide dielectric surface following CMP and to remove residual slurry particles from a combined silicon dioxide and silicon nitride dielectric surface following shallow trench isolation (STI) planarization. Both silicon dioxide and silicon nitride are hydrophilic. However, when silicon is exposed following a CMP process, a hydrophobic (i.e., water-repelling) surface is created, which makes it difficult to use aqueous NH_4OH -based scrubbing. The silicon surface does not sufficiently wet to permit the polyvinyl alcohol brushes coming into intimate contact with the wafer surface, and the residual slurry particles and/or metal contaminants are not removed.

An object of the invention, then, is to provide a wafer surface comprising semiconductor and dielectric that attracts enough water to allow the wafer surface to wet so that residual slurry particles and metal contaminants may be removed therefrom.

To address the Examiner's concerns in turn:

It is not known what is the width that 'a first width' [is] referring to.

The characteristics of the first width is defined in the claim: "... the first width ensuring that the surface of the wafer can attract enough water to wet sufficiently allowing removal of residual particles therefrom ...". This is a functional limitation, as discussed in MPEP 2173.05(g). Aspects of the invention provide for semiconductor regions disposed between dielectric regions. The "first width" is thus a width of the

semiconductor regions that will render the overall surface sufficiently hydrophilic to be cleanable. Dependent claims (e.g. claims 4 and 5) claim actual values for the first width. A more fully elaborated discussion of the "first width" appears in the specification at paragraph [0018]:

The shortest dimension of each region of hydrophobic material is less than or equal to a first width (e.g., 500 μm), so that the regions of hydrophobic material are not too large. The first fraction and the first width limit the size as well as the density of the regions of hydrophobic material to prevent the wafer surface as a whole from becoming hydrophobic. The first fraction and the first width ensure that there is enough hydrophilic material at the wafer surface among the regions of hydrophobic material so that the attractive forces inherent in the hydrophilic material counteract the repulsive forces inherent in the hydrophobic material. Hydrophobicity can be measured by contact angle measurements. A surface is considered hydrophilic when the contact angle measurements following CMP are most preferably less than 5 degrees, preferably less than 10 degrees, but acceptable if less than 15 degrees.

The Examiner's concerns continue:

Should the first width be the width of the wafer or the width of the semiconductor regions or the width of the dielectric regions?

On this point Applicants cannot find ambiguity in the language of the claim: "... each of the polysilicon semiconductor regions have a shortest surface dimension that is less than or equal to a first width ..." The "first width" is the width of the shortest dimension of the polysilicon semiconductor regions. Applicants are unable to envision a reading of this claim in which the first width could refer to the width of either the wafer or of the dielectric regions.

Moreover, Applicants respectfully point out that this "first width" language with its associated qualifiers appears in claims 1, 30, and 44 as originally filed on February 2, 2001, and has been unchanged by intervening amendments. This Examiner has issued two previous Office Actions without raising either formal or informal objections to the same wording which is here rejected under 35 USC 112. Applicants are puzzled that language previously considered acceptable is deemed indefinite in the latest Office Action.

D. 35 USC 102 Rejections: Crafts et al.

Claims 1, 7, 8, 11, 12, 14, 30, 36, 38, 39, 41, 43, 44, 50, 53, 54, and 60-62 were rejected under 35 USC 102(b) as anticipated by Crafts et al., US Patent No. 5,920,110.

As amended, claim 1 recites a wafer having a surface, the wafer comprising a plurality of regions of dielectric and polysilicon semiconductor exposed at the surface of the wafer after chemical mechanical planarization, the polysilicon semiconductor regions formed over a substrate, wherein the polysilicon semiconductor regions have a total surface area that is less than or equal to a first fraction of a total surface area of the wafer and each of the polysilicon semiconductor regions have a shortest surface dimension that is less than or equal to a first width, the first fraction and the first width ensuring that the surface of the wafer can attract enough water to wet sufficiently allowing removal of residual particles therefrom, and wherein the surface is planarized.

The Examiner points to Fig. 7D of Crafts et al., citing polysilicon regions formed by layers 54, 56, and 58 and separated by dielectric regions 62. The Examiner finds the surface of regions 62 and 58, presumed to exist before regions 63 are formed, to anticipate claim 1.

Applicants believe, however, that several limitations of the claim do not appear in the surface of Crafts et al. This surface does in fact contain a plurality of regions of dielectric and polysilicon semiconductor. However, a) the dielectric and semiconductor regions of Crafts et al. are not "exposed at the surface of the wafer after chemical mechanical planarization," b) the semiconductor regions of Crafts et al. do not have "a total surface area that is less than or equal to a first fraction of a total surface area of the wafer and each of the polysilicon semiconductor regions have a shortest surface dimension that is less than or equal to a first width, the first fraction and the first width ensuring that the surface of the wafer can attract enough water to wet sufficiently allowing removal of residual particles therefrom," and c) the surface of Crafts is not planarized.

Taking each point in turn:

a) **"exposed ... after chemical mechanical planarization ..."** In the present invention, the regions at the surface of the present invention are exposed by chemical mechanical planarization. In contrast, no chemical mechanical planarization, or indeed

any planarizing mechanism at all, is described or suggested by Crafts et al. The Examiner proposes to discount this limitation:

The expressions "after chemical mechanical planarization" ... [is] taken to be a product by process limitation and is given no patentable weight ... it is the patentability of the final structure "gleaned" from the process steps which must be determined in a "product by process" claim, and not the patentability of the process

It is evident that a surface exposed after chemical mechanical planarization is measurably and qualitatively different from a surface that has *not* been exposed after chemical mechanical planarization; i.e. that the "product 'gleaned' from the process steps" is clearly not the same if the planarizing step is omitted.

To summarize, a CMP-planarized surface and a non-CMP-planarized surface are not the same. Since the present invention relates to a method to clean a surface after CMP, this difference cannot be considered incidental or unimportant.

b) "...wherein the polysilicon semiconductor regions have a total surface area that is less than or equal to a first fraction of a total surface area of the wafer and each of the polysilicon semiconductor regions have a shortest surface dimension that is less than or equal to a first width, the first fraction and the first width ensuring that the surface of the wafer can attract enough water to wet sufficiently allowing removal of residual particles therefrom ..."

The Examiner states:

With respect to the limitation "the polysilicon semiconductor regions have a total surface area that is less than or equal to a first fraction of a total surface area of the wafer", the polysilicon island (40, top view) has a total surface area (see Fig. 6), thus, the limitation of the claim is met.

The Examiner has quoted only a portion of a limitation, not the entire limitation; clearly Applicants do not intend to limit semiconductor regions to those having an area, as a region with no area is a logical impossibility.

With respect to the limitation "each of the polysilicon semiconductor regions have a shortest surface dimension that is less than or equal to a first width", since the polysilicon semiconductor region (58) of Crafts has a surface dimension and the "first width" is not defined, thus the limitation of the claim is met.

The Examiner has again quoted only a portion of a limitation, not the entire limitation; clearly Applicants do not intend to limit semiconductor regions to those having a shortest dimension. As described in section C of these Remarks, the response in this paper to the 35 USC 112 rejection, the term "first width" is not undefined or indefinite. The Examiner continues:

With respect to the functional limitation: "the first fraction and the first width ensuring that the surface of the wafer can attract enough water to wet sufficiently allowing removal of residual particles therefrom," since the polysilicon semiconductor regions (58) have a total surface area that is less than or equal to an unspecified first fraction, and the first width is undefined, thus, the wafer having a surface of Crafts should inherently function as claimed.

As described throughout the specification and claims of the present invention, it is the *relationship* between the area of the hydrophobic semiconductor regions and the area of the hydrophilic dielectric regions, and the shortest surface dimension of the semiconductor regions, that determine whether or not the overall surface of the wafer is wettable, and thus cleanable, after CMP. There is no reason to assume the semiconductor and dielectric regions at the surface of Crafts et al. would have a relationship or size causing them to have this property. The term "first fraction" is not unspecified for the same reasons that the term "first width" is not undefined; see the discussion of the 35 USC 112 rejection in section C of these Remarks.

c) "...wherein the surface is planarized." As amended, claims 1, 30, and 44 recite that the surface is planarized. As noted above, a planarized surface is measurably and quantitatively different from an unplanarized surface; thus this limitation cannot be dismissed as a process step irrelevant to the final product. There is no description or suggestion of a planarizing step in Crafts et al. In fact, several aspects of the description suggest absence of a planarizing step.

The dielectric fill is described as spin-on-glass (col. 15, line 62). Due to surface tension, spin-on-glass can be deposited in gaps between semiconductor regions without covering the semiconductor regions, so planarization is not necessarily required. No provision is made in Crafts et al. to deposit extra thickness of semiconductor, allowing for some to be lost during planarization (the present invention describes this loss of thickness, for example in paragraph [0031].) There is no mention in Crafts et al. of the

need for planarity of this layer. Planarizing at such a stage was not standard at the time of the original filing date of the specification of Crafts et al., and one skilled in the art would have no reason to assume any such step was performed.

Independent claims 30 and 44 were rejected using the same rationale as independent claim 1, and thus the same logic applies.

Applicants have shown that Crafts et al. fail to teach each and every limitation of the claims, and thus request the 102(b) rejection of independent claims 1, 30, and 44 and their dependent claims 7, 8, 11, 12, 14, 36, 38, 39, 41, 43, 50, 51, 53, 54, and 60-62 be withdrawn.

Applicants note that the Examiner's actual rejection reads as follows:

Claims 1, 7, 8 ... are rejected under 35 USC 102(b) as anticipated by
or, in the alternative, under 35 USC 103(a) as obvious over Crafts et al.
...

The remainder of the rejection appears in the form of a 35 USC 102 rejection. There is no motivation to modify the reference identified, nor indeed any modification suggested, as is typical in a 103 rejection. It is Applicants' intention to craft a fully responsive reply, but with no clear 103 rejection spelled out, Applicants are unable to respond to it.

E. 35 USC 102 Rejections: Liu et al.

Claims 1, 9, 10, 30, 37, 40, 44, and 52 were rejected under 35 USC 102(b) as anticipated by Liu et al., US Patent No. 5,612,914.

With respect to claims 1, 30, and 44, the Examiner writes:

"With respect to: the first width, the first fraction, the sufficiently wet
and Product-by-process limitation, a similar reasoning as that of claim
1 is also applied here.

The reasoning detailed in section D of these Remarks, in the response to the 102(b) rejections using the Crafts et al. reference, thus also apply here.

Applicants have shown that Liu et al. fail to teach each and every limitation of the claims, and thus request the 102(b) rejection of independent claims 1, 30, and 44 and their dependent claims 9, 10, 37, 40, and 52 be withdrawn.

Applicants note that the Examiner's actual rejection reads as follows:

Claims 1, 9, 10 ... are further rejected under 35 USC 102(b) as anticipated by or, in the alternative, under 35 USC 103(a) as obvious over Liu et al. ...

The remainder of the rejection appears in the form of a 35 USC 102 rejection. There is no motivation to modify the reference identified, nor indeed any modification suggested, as is typical in a 103 rejection. It is Applicants' intention to craft a fully responsive reply, but with no clear 103 rejection spelled out, Applicants are unable to respond to it.

F. 35 USC 103 Rejections: Crafts et al.

Claims 2-5, 31-34, and 45-48 were rejected under 35 USC 103(a) as being unpatentable over Crafts et al.

Claim 1 recites a wafer having a surface, the wafer comprising a plurality of regions of dielectric and polysilicon semiconductor exposed at the surface of the wafer after chemical mechanical planarization, the polysilicon semiconductor regions formed over a substrate, wherein the polysilicon semiconductor regions have a total surface area that is less than or equal to a first fraction of a total surface area of the wafer and each of the polysilicon semiconductor regions have a shortest surface dimension that is less than or equal to a first width, the first fraction and the first width ensuring that the surface of the wafer can attract enough water to wet sufficiently allowing removal of residual particles therefrom, and wherein the surface is planarized. Claim 2 adds the limitation that the first fraction equals 60%; claim 3 that the first fraction equals 50%.

Regarding claims 2, 31, 45, 3, 32, and 46, the Examiner writes:

Thus, Crafts is shown to teach all the features of the claim with the exception of explicitly disclosing the first fraction to be 50% or 60% of the total surface area of the wafer. The claimed fractions do not appear to be critical.

Note that the specification contains no disclosure of either the *critical nature of the first fractions* [or] *of any unexpected results arising therefrom*.

As detailed in section D of these Remarks, Applicants do not agree that the surface of Crafts et al. teaches all of the features of claims 2, 3, 31, 32, 45, and 46 with the exception of the wafer surface percentage. In addition, Applicants cannot agree that

the specification contains no disclosure of the critical nature of the values that appear in these claims. Paragraph [0018] of the specification of the present invention states:

... The first fraction and the first width limit the size as well as the density of the regions of hydrophobic material to prevent the wafer surface as a whole from becoming hydrophobic. The first fraction and the first width ensure that there is enough hydrophilic material at the wafer surface among the regions of hydrophobic material so that the attractive forces inherent in the hydrophilic material counteract the repulsive forces inherent in the hydrophobic material.

Paragraph [0021] spells out some specific values that satisfy these requirements:

The first fraction is most preferably 50%, preferably 60%, but may be 70%. In the example shown in FIGS. 1A-1B, semiconductor is about 57% of the surface area of wafer 10 and dielectric is about 43%.

This description makes clear that the fractions are critical, and provides specific examples. The Examiner continues:

... one having ordinary skill in the art would have concluded that the polysilicon semiconductor regions (58) (shown as islands 40, within the dielectric regions 62, blank area, in fig. 6) have a total surface area which is less than 50% of the total surface area of the wafer.

Applicants point out that whether one skilled in the art, studying Fig. 6 of Crafts et al., would have concluded the total surface area of the polysilicon islands 40 of Fig. 6 of Crafts et al. is or is not 50%, is not relevant. What matters is whether one skilled in the art would have determined that 50% was an obvious first fraction of the wafer surface made up of polysilicon semiconductor regions in order for resulting planarized surface to be wettable, and thus cleanable. As CMP planarization was not standard at the time the specification of Crafts et al. was written, such a conclusion would certainly not have been obvious.

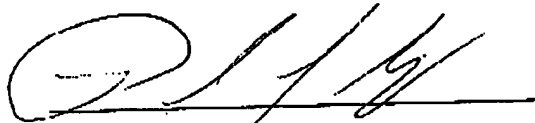
Applicants have shown that the criticality of the fractions in the rejected claims is in fact shown in the specification, and further that Crafts et al. fail to teach each and every limitation of the rejected claim, and thus request that the 35 USC 103 rejection of the claims be withdrawn.

CONCLUSION

In view of these amendments and remarks, Applicants submit that this application is in condition for allowance. **If any objections or rejections remain, Applicants respectfully request an interview to discuss the references.** In such event, the Examiner is asked to contact the undersigned agent at (408) 869-2921.

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Date



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